AGILENT TECHNOLOGIES
Legal Department, M/S DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599

PATENT APPLICATION
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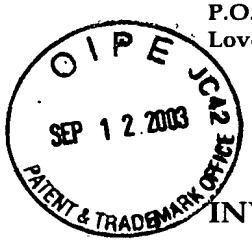

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTOR(S): Que-Won Rhee **CONFIRMATION NO:** 1594

SERIAL NO: 09/432,819 **GROUP ART UNIT:** 2182

FILED: November 2, 1999 **EXAMINER:** Ilwoo Park

SUBJECT: CONFIGURABLE ARCHITECTURE FOR VIRTUAL SOCKET CLIENT TO AN ON-CHIP BUS INTERFACE BLOCK

ASSISTANT COMMISSIONER OF PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

REPLY BRIEF

Appellant herein replies to new points raised in the Examiner's Answer for the above-identified case.

GROUPING OF CLAIMS

The Examiner has argued that the rejection of claims stand or fall together because Appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. Appellant respectfully traverses this argument by Examiner.

37 CFR 1.192(C)(7) states the following:

> For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a

> statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

Appellant has included a statement that the rejected claims do not stand or fall together. Additionally, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of each group are believed to be separately patentable. Appellant has not merely pointing out differences in what the claims cover, but for each group has provided an argument as to why the claims in the group are separately patentable over USPN 5,870,310) *Malladi.*

Specifically, under the Section titled "Grouping of Claims" of the Appeal Brief, Appellant included the following statement: "The rejected claims do not stand or fall together."

Under the Section titled "Argument" of the Appeal Brief, Appellant provided arguments for each group as to why the group is separately patentable over *Malladi.* Specifically, for every claim group, Appellant set out subject matter for that claim group that was not disclosed or suggested by *Malladi* and discussed errors made by the Examiner in the stated rationale for the rejection.

For example, in the section entitled "C. Discussion of Group 1 claim (claim 1)", Appellant pointed out errors made in the rejection and

clearly pointed out subject matter within independent claim 1 that is not found either expressly or inherently in *Malladi*.

In the section entitled "D. Discussion of Group 2 claim (claim 2)", Appellant pointed out subject matter within dependent claim 2 that is not found either expressly or inherently in *Malladi* (and is also not found in independent claim 1). Appellant also pointed out errors made by the Examiner in the stated rationale for the rejection. This discussion of Group 2 claim did not merely point out differences in what claim 2 covered, vis-à-vis claim 1, but was a complete argument as to why additional subject matter set out in claim 2 made claim 2 separately patentable over *Malladi*.

Appellant continued the same pattern for each claim group. That is, for each claim group, Appellant set out subject matter in that claim group that was not disclosed or suggested by *Malladi* and pointed out errors made by the Examiner in the stated rationale for the rejection.

ARGUMENT

New Point Raised by the Examiner:

In the Examiner's Answer, on page 9, Footnote 2, Examiner has argued:

> Each of shells/cores/cells is a module because each of them is stored in the library as a unit or module [col. 1, lines 41-65], can be selected or re-useable [col. 5, lines 28-35] as needed [col.5, lines 2-9].

Appellant's Response:

Examiner appears to be arguing that interface logic cells are modular because they are stored in a library and can be reused. This definition for "modular" given by Examiner does not agree with the way the word modular is used by Appellant or with the general usage of the word.

Modular can be defined as "made up of separate modules that can be rearranged, replaced, or interchanged easily." See Encarta® World English Dictionary © 1999 Microsoft Corporation. All rights reserved. Developed for Microsoft by Bloomsbury Publishing Plc.

Thus, when Appellant pointed out that nothing in *Malladi* discloses or suggests that the interface logic cells are modular, Appellant was arguing that nothing in *Malladi* discloses or suggests that the interface logic cells are made up of separate modules.

Examiner has seemingly responded by arguing that the logic cell itself is a logic module of an integrated circuit. Nevertheless, this does not disclose or suggest that the logic cell, itself, is composed or made up of separate modules.

Claim 1, for example, states that an interface block comprises a synchronization module, a translation module, a queue module, and a driver module.

Examiner has failed to show that the interface logic cells (or any equivalent to an interface block within *Malladi*) are modular (i.e., are made up of separate modules). Further, nothing in *Malladi* discloses or suggests the particular modules (a synchronization module, a translation module, a queue module and a driver module) set out by claim 1 being included within a single interface block, as set out in claim 1.

New Point Raised by the Examiner:

In the Examiner's Answer, on page 9, lines 10 through 16, Examiner has argued:

> *Malladi* teaches, for example a synchronization module [e.g., MIU 150a] and a driver [BIU 140a] are within the same interface block [shell 141a] and interface to the same bus [CPU bus 100], a synchronization module [e.g., MIU 150b] and a driver [BIU 140b] are within the same interface block [shell 141b] and interface to the same bus [CPU bus 100], a synchronization module [e.g., MIU 336] and a driver [BIU 340] are within the same interface block [shell 337] and interface to the same bus [CPU bus 316],

Appellant's Response:

Examiner has clearly misread *Malladi*. For example, Examiner asserts that MIU 150a interfaces with CPU bus 100. This is clearly wrong. From Figure 1, it is clearly seen that MIU 150a interfaces with memory bus 102. MIU 150a does not interface with CPU bus 100.

As is clear from Figure 1, MIU 150a provides a complete interface between memory bus 102 and data processing core 108. BIU 140a provides a complete interface between CPU bus 100 and data processing core 108. While MIU 150a and BIU 140a are both within shell 141a, they clearly do not interface to the same bus.

Likewise, Examiner asserts that MIU 150b interfaces with CPU bus 100. This is clearly wrong. From Figure 1, it is clearly seen that MIU 150b interfaces with memory bus 102. MIU 150b does not interface with CPU bus 100.

As is clear from Figure 1, MIU 150b provides a complete interface between memory bus 102 and data processing core 108. BIU 140b provides a complete interface between CPU bus 100 and data processing core 108. While MIU 150b and BIU 140b are both within shell 141b, they clearly do not interface to the same bus.

Likewise, Examiner asserts that MIU 336 interfaces with CPU bus 316. This is clearly wrong. From Figure 1, it is clearly seen that MIU 336 interfaces with memory bus 314. MIU 336 does not interface with CPU bus 316.

As is clear from Figure 1, MIU 336 provides an interface between memory bus 314 and pre-fetch buffer 338. BIU 340 provides a interface between CPU bus 316 and both input RAM 342 and pre-fetch buffer 338. While MIU 336 and BIU 340 are both within audio shell 337, they clearly do not interface to the same bus.

Claim 1 states that an interface block between an internal bus and a socket of a logic block includes a synchronization module and a driver module. The examples that the Examiner gives from *Malladi* of a "synchronization module" (e.g., MIUs 150a-150c) and a "driver module" (e.g., BIUs 140a-140c) do not even interface to the same bus. That is, MIUs 150a-150c interface to memory bus 102 and BIUs 140a-140c interface to CPU bus 100.

New Point Raised by the Examiner:

In the Examiner's Answer, on page 10, line 17 through page 11, line 3, Examiner has argued:

> *Malladi* teaches an interface block that comprises a plurality of modules [e.g., logic cells 140a, 108, 150a inside of shell 141a, logic cells 140b, 110, 150b inside of shell 141b, logic cells 240b, 110, 250b inside of shell 141b', logic cells 302, 304,308 inside of shell 301, logic cells 3002, 306, 312 inside of shell 301, logic cells 310, 306, 312 inside of shell 301 [....]] connected in series

Appellant's Response:

Examiner has set out a number of entities within *Malladi* connected in series. For example, Examiner has correctly stated that BIU 140a, data processing core 108, and MIU 150a are connected in series. Likewise, BIU 140b, data processing core 110, and MIU 150b are connected in series. And so on.

However, these entities, connected in series, pointed out by Examiner, are not in any way similar to the plurality of modules connected in series set out in claim 7.

Specifically, in claim 7, the plurality of modules connected in series are part of an interface block that provides an interface between an internal bus of the integrated circuit and a socket of a logic block.

BIU 140a, data processing core 108, and MIU 150a, for example, are not part of an interface block that provides an interface between an internal bus of the integrated circuit and a socket of a logic block. Likewise BIU 140b, data processing core 110, and MIU 150b are not part of an interface block that provides an interface between an internal bus of the integrated circuit and a socket of a logic block. And so on.

Further, claim 7 sets out that each module in the plurality of modules performs only a single function from a plurality of functions. Any needed synchronization between a clock domain of the internal bus and a clock domain of the socket of the logic block is a first function from the plurality of functions. Any required translation of block encoding of data is a second

function from the plurality of functions. Any buffering of data flowing between the internal bus and the socket of the logic block is a third function from the plurality of functions. Handling any low level and electrical drive specifications of the internal bus is a fourth function from the plurality of functions.

In *Malladi*, there is no such division of functions among, for example, between BIU 140a, data processing core 108, and MIU 150a or between BIU 140b, data processing core 110, and MIU 150b. These elements are nothing at all like the modules described in claim 7.

CONCLUSION

For all the reasons set out in the Appeal Brief, Appellant believes the rejection of the claims was in error and respectfully requests that the rejection be reversed.

Respectfully submitted,
QUE-WON RHEE

By _____
Douglas L. Weller
Reg. No. 30,506

September 8, 2003
Santa Clara, California
(408) 985-0642